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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,004	10/02/2003	Thomas J. Ribarich	IR-2171 (2-3689)	9223

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EXAMINER	
SAWHNEY, HARGOBIND S	

ART UNIT	PAPER NUMBER
2875	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,004	RIBARICH, THOMAS J.	
	Examiner	Art Unit	
	Hargobind S Sawhney	2875	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 38-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 38-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/6/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on August 30, 2004 has been entered. Accordingly:

- Claims 17-37 have been cancelled; and
- Claims 1, 9, 38 and 42 have been amended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-15 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishio et al. (US Patent No.: 6,437,502 B1) in view of Nomoto et al. (US Patent No.: 4,739,222).

Regarding claim 1, Nishio et al. ('502 B1) discloses a compact florescent lamp package 10 (Figure 1, column 11, lines 18 and 19) comprising:

- a base 12 electrically connectable to the electrical socket capable for receiving an ordinary incandescent lamp (Figure 1, column 11, line 20);
- the base 12 including an open end, a closed end and a wall enclosing space (Figure 1);

- a multi-chip module 16 including a ballast circuit on a circuit board 24 (Figures 1 and 7, column 11, line 20, and column 15, lines 45-55);
- the multi-chip module being contained entirely within the space defined in the base 12 (Figure 1), and the muti-chip module being electrically connected to the base with the element 25 (Figure 1); and
- a fluorescent lamp 18 extending away from the base 12 (Figure 1), and operatively connected to the ballast circuit included in the ballast circuit 24 (Figures 1 and 3, column 14, lines 43-47).

However, Nishio et al. ('502 B1) does not specifically teach a thermally conductive body disposed within the base, and further thermally connecting to said ballast circuit.

On the other hand, Nomoto et al. ('222) disclose a compact fluorescent lamp package (Figures 1A, 1B, 3A and 3B) comprising a base 1 housing electronic elements including 5 and 7 (Figures 1A, 1B, 3A and 3B, column 2, lines 50, and column 3, lines 32 and 33). Nomoto et al. ('222) further teaches the cavity space of the base including thermal epoxy for mechanical stability and thermal management (Figures 1A, 1B, 3A and 3B, column 2, lines 4-13 and 65-68).

It would be have been obvious to one of ordinary skill in the art at the time of the invention to modify the compact Fluorescent lamp package of Nishio et al. ('502 B1) by filling thermal epoxy compound as taught by Nomoto et al. ('222) for benefit and advantage of efficient transfer of heat generated during operation to the outer casing, and thus improving efficiency and operational life of the device.

Regarding claims 2-15, Nishio et al. ('502 B1) in view of Nomoto et al. ('222) discloses the compact florescent lamp package 10 (Figure 1, column 11, lines 18 and 19) comprising:

- a diffuser cover 17 enveloping the fluorescent lamp 18, and providing appearance of an ordinary incandescent lamp (Nishio, Figure 1, column 11, line 21);
- the base 12 being an Edison screw base (Nishio, Figure 1, column 11, lines 39 and 40);
- the multi-chip module 16 being mounted on a single circuit board (Nishio, Figure 1)
- the ballast circuit elements including 25 and 26 being mounted on both sides of the circuit board 24 (Nishio, Figure 1, column 11, lines 57-59);
- the design independent electronic components including power switching devices – diode bridge, rectifiers etc. – being mounted on one side of the circuit board 24 (Nishio, Figure 1, column 11, line 67, and column 12, lines 1-3);
- the design dependent electronic components, including capacitors, being mounted on another, opposing, side of the circuit board 24 (Nishio, Figure 1, column 11, lines 63-67);
- the heat –conducting body being a thermal epoxy disposed in the base 2 (Nomoto, Figures 1A, 1B, 3A and 3B, column 2, lines 4-13 and 65-68);

- the multi-chip module 16 formed on a circular circuit board having its parameter following the contour of the walls of the base 12 (Nomoto, Figures 1 and 12);
- the multi-chip module 16 formed on a generally polygonal circuit board (Nomoto, Figure 1, column 18, lines 24-28);
- the wall of the base 12 inherently serving as a connector connecting the lamp to first pole of a power line; and the closed end of the base inherently insulated from the wall, and connecting to the second pole of the power line (Nomoto, Figures 1,3 and 8);
- the multi-chip module 16 being electrically connected to the end connector via a second electrical wire 25 (Nomoto, Figures 1 and 3); further the multi-chip module 16 being electrically connected to the wall of the base with a first wire (not shown) operationally required to close the circuit (Nomoto, Figures 1 and 3); and
- the fluorescent lamp 18 being connected to the multi-chip module 16 via respective filament terminals 48 (Nomoto, Figures 1 and 3, column 14, lines 43-47).

Regarding claim 38, Nishio et al. ('502 B1) discloses a compact florescent lamp package 10 (Figure 1, column 11, lines 18 and 19) comprising:

- a base 12 electrically receivable to the electrical socket capable (Figure 1, column 11, line 20);

- the base 12 including an open end, a closed end and a wall enclosing the defined space (Figure 1);
- the base 12 connectable to an external electrical connection (Figure 1);
- a circuit board
- the circuit board 16 having two opposing surfaces disposed in the space confined in the base 12, including element 14, (Nishio, Figure 1)
- the ballast circuit elements including 25 and 26 being mounted on both sides of the circuit board 24 (Nishio, Figure 1, column 11, lines 57-59);
- the ballast circuit elements including 25 and 26 electrically connected to the base 12, via element 25 (Nishio, Figure 1);
- a fluorescent lamp 18 extending away from the base 12 (Figure 1), and operatively connected to the ballast circuit included in the ballast circuit 24 (Nishio, Figures 1 and 3, column 14, lines 43-47); and
- a diffuser cover 17 enveloping the fluorescent lamp 18, and providing appearance of an ordinary incandescent lamp (Nishio, Figure 1, column 11, line 21).

However, Nishio et al. ('502 B1) does not specifically teach a thermally conductive body disposed within the base, and further thermally connecting the base to said ballast circuit.

On the other hand, Nomoto et al. ('222) disclose a compact fluorescent lamp package (Figures 1A, 1B, 3A and 3B) comprising a base 1 housing electronic elements including 5 and 7 (Figures 1A, 1B, 3A and 3B, column 2, lines 50, and column 3, lines

32 and 33). Nomoto et al. ('222) further teaches the cavity space of the base including thermal epoxy for mechanical stability and thermal management (Figures 1A, 1B, 3A and 3B, column 2, lines 4-13 and 65-68).

It would be have been obvious to one of ordinary skill in the art at the time of the invention to modify the compact Fluorescent lamp package of Nishio et al. ('502 B1) by filling thermal epoxy compound as taught by Nomoto et al. ('222) for benefit and advantage of efficient transfer of heat generated during operation to the outer casing, and thus improving efficiency and operational life of the device.

Regarding claims 39-42, Nishio et al. ('502 B1) in view of Nomoto et al. ('222) meets the limitations in similar manner as that detailed above for the rejections of claims 4, 2, 1 and 9 respectively.

4. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishio et al. (US Patent No.: 6,437,502 B1) in view of Nomoto et al. ('222) as applied to Claim 1 above, and in view of Matsushita (Japanese Patent No.: JP 11025751 A).

Nishio et al. ('502 B1) in view of Nomoto et al. ('222) discloses a compact Fluorescent lamp package comprising a base housing a multi-chip module including a ballast circuit on a circuit board. However, neither combined nor individual teaching Nishio et al. ('502 B1) and Nomoto et al. ('222) specifically teaches the circuit including a heat sink disposed on one of the major surfaces of the circuit board.

On the other hand, Matsushita (Japanese Patent No.: JP 11025751 A) discloses a heat dissipation structure of a fluorescent lamp lighting system comprising a circuit

board 3 having a heat sink 4 mounted on its one of the major surfaces (Figure 1, English translated abstract).

It would be have been obvious to one of ordinary skill in the art at the time of the invention to modify the compact Fluorescent lamp package of Nishio et al. ('502 B1) in view of Nomoto et al. ('222) by providing heat sink as taught by Matsushita (Japanese Patent No.: JP 11025751 A) for the advantages and benefits of preventing operational losses and component replacements due to radiant heat of the lamp.

Response to Amendment

5. Applicant's arguments filed on August 30,2004 with respect to the 35 U.S.C. 102(e) rejection of claims 1 and 38 have been fully considered but they are not persuasive.

Argument: Nishio et al. ('502 B1) in view of Nomoto et al. ('222) teaches a thermal conductive body in contact with the outer casing, and not base portion as claimed by the applicant.. Therefore, Nishio et al. ('502 B1) in view of Nomoto et al. ('222) does not meet the limitations of claims 1 and 38.

Response: As detailed above, Nomoto et al. ('222) further teaches the cavity space of the base including thermal epoxy in contact with the base 1, as well as with the heat producing electronic component including transformer and its circuitry, for mechanical stability and

thermal management (Figures 1A, 1B, 3A and 3B, column 2, lines 4-13 and 65-68).

It would be have been obvious to one of ordinary skill in the art at the time of the invention to modify the compact Fluorescent lamp package of Nishio et al. ('502 B1) by filling thermal epoxy compound between the base and the circuit board as taught by Nomoto et al. ('222) for benefit and advantage of efficient transfer of heat generated during operation to the outer casing, and thus improving efficiency and operational life of the device.

Therefore, Nishio et al. ('502 B1) in view of Nomoto et al. ('222) meets the limitations of claims 1 and 38.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hargobind S Sawhney whose telephone number is 571 272 2380. The examiner can normally be reached on 6:15 - 2:45.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sandra O'Shea can be reached on 571-272-2378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HSS
11/23/2004

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